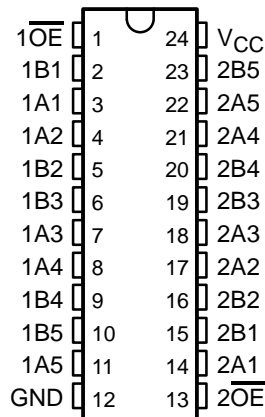- **5-Ω Switch Connection Between Two Ports**
- **TTL-Compatible Input Levels**
- **Designed to Be Used in Level-Shifting Applications**
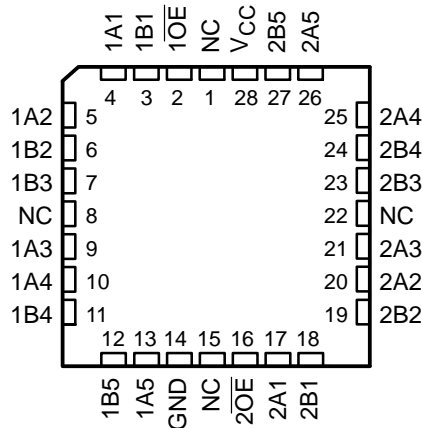
description/ordering information

The 'CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

These devices are organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

SN54CBTD3384 . . . JT OR W PACKAGE
SN74CBTD3384 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		24	V_{CC}
1B1	2		23	2B5
1A1	3		22	2A5
1A2	4		21	2A4
1B2	5		20	2B4
1B3	6		19	2B3
1A3	7		18	2A3
1A4	8		17	2A2
1B4	9		16	2B2
1B5	10		15	2B1
1A5	11		14	2A1
GND	12		13	2$\overline{OE}$

SN54CBTD3384 . . . FK PACKAGE
(TOP VIEW)

Top pins: 1A1, 1B1, 1$\overline{OE}$, NC, V_{CC}, 2B5, 2A5 (4 3 2 1 28 27 26)

1A2	5	25	2A4
1B2	6	24	2B4
1B3	7	23	2B3
NC	8	22	NC
1A3	9	21	2A3
1A4	10	20	2A2
1B4	11	19	2B2

Bottom pins: 1B5, 1A5, GND, NC, 2$\overline{OE}$, 2A1, 2B1 (12 13 14 15 16 17 18)

NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – DW	Tube	SN74CBTD3384DW	CBTD3384
		Tape and reel	SN74CBTD3384DWR	
	SSOP – DB	Tape and reel	SN74CBTD3384DBR	CC384
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3384DBQR	CBTD3384
	TSSOP – PW	Tape and reel	SN74CBTD3384PWR	CC384
	TVSOP – DGV	Tape and reel	SN74CBTD3384DGVR	CC384
−55°C to 125°C	CDIP – JT	Tube	SNJ54CBTD3384JT	SNJ54CBTD3384JT
	CFP – W	Tube	SNJ54CBTD3384W	SNJ54CBTD3384W
	LCCC – FK	Tube	SNJ54CBTD3384FK	SNJ54CBTD3384FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
1$\overline{\text{OE}}$	2$\overline{\text{OE}}$	1B1–1B5	2B1–2B5
L	L	1A1–1A5	2A1–2A5
L	H	1A1–1A5	Z
H	L	Z	2A1–2A5
H	H	Z	Z

logic diagram (positive logic)
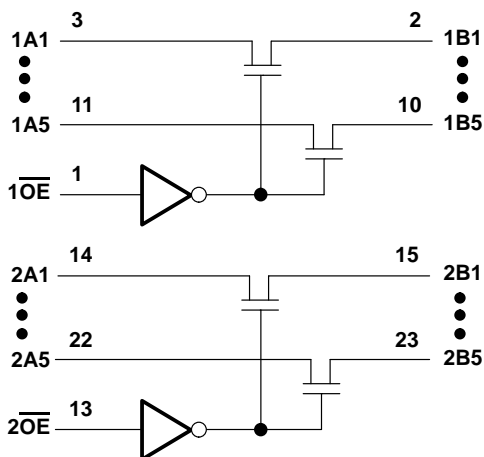
Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O}$ < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

![Texas Instruments logo]
TEXAS
INSTRUMENTS

recommended operating conditions (see Note 3)

		SN54CBTD3384		SN74CBTD3384		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level control input voltage	2		2		V
V_{IL}	Low-level control input voltage		0.8		0.8	V
T_A	Operating free-air temperature	−55	125	−40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54CBTD3384			SN74CBTD3384			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		See Figure 2								
I_I		V_{CC} = 5.5 V, V_I = 5.5 V or GND				±1			±1	μA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND				1.5			1.5	mA
ΔI_{CC}‡	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				2.5			2.5	mA
C_i	Control inputs	V_I = 3 V or 0			3			3		pF
$C_{io(OFF)}$		V_O = 3 V or 0, $\overline{OE}$ = V_{CC}			3.5			3.5		pF
r_{on}§		V_{CC} = 4.5 V	V_I = 0	I_I = 64 mA	5			5		7	Ω
				I_I = 30 mA	5			5		7	
			V_I = 2.4 V,	I_I = 15 mA	35			35		50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)
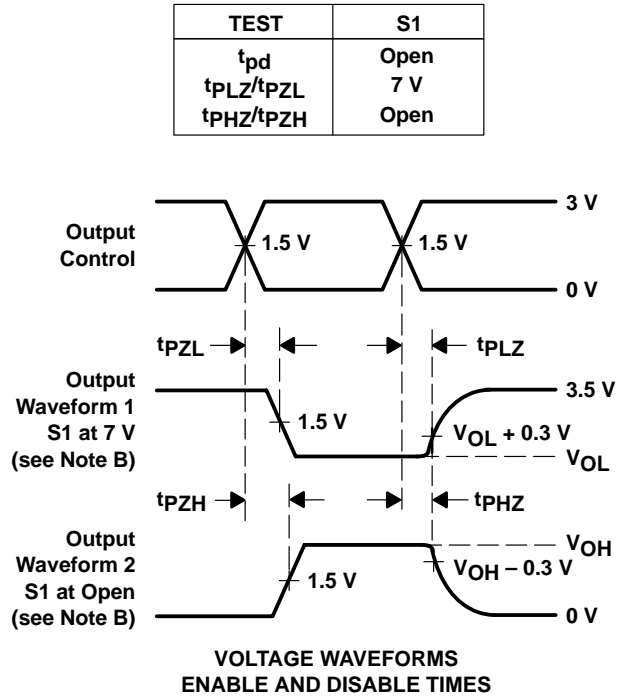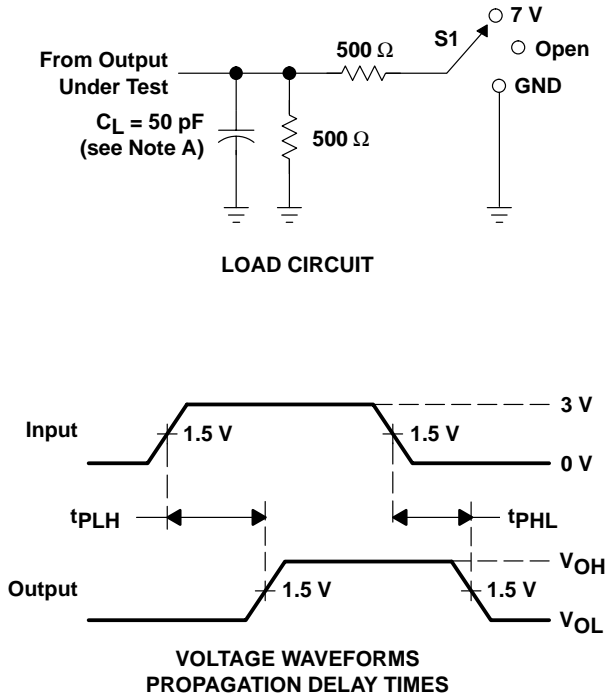
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBTD3384		SN74CBTD3384		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}¶	A or B	B or A		0.25		0.25	ns
t_{en}	$\overline{OE}$	A or B	2.2	9.7	2.3	7	ns
t_{dis}	$\overline{OE}$	A or B	1.5	8.6	1.7	5.3	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

TEXAS
INSTRUMENTS

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
　　　　B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
　　　　　 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
　　　　C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ \Omega$, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns.
　　　　D. The outputs are measured one at a time with one transition per measurement.
　　　　E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
　　　　F. t_{PZL} and t_{PZH} are the same as t_{en}.
　　　　G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

OUTPUT VOLTAGE HIGH
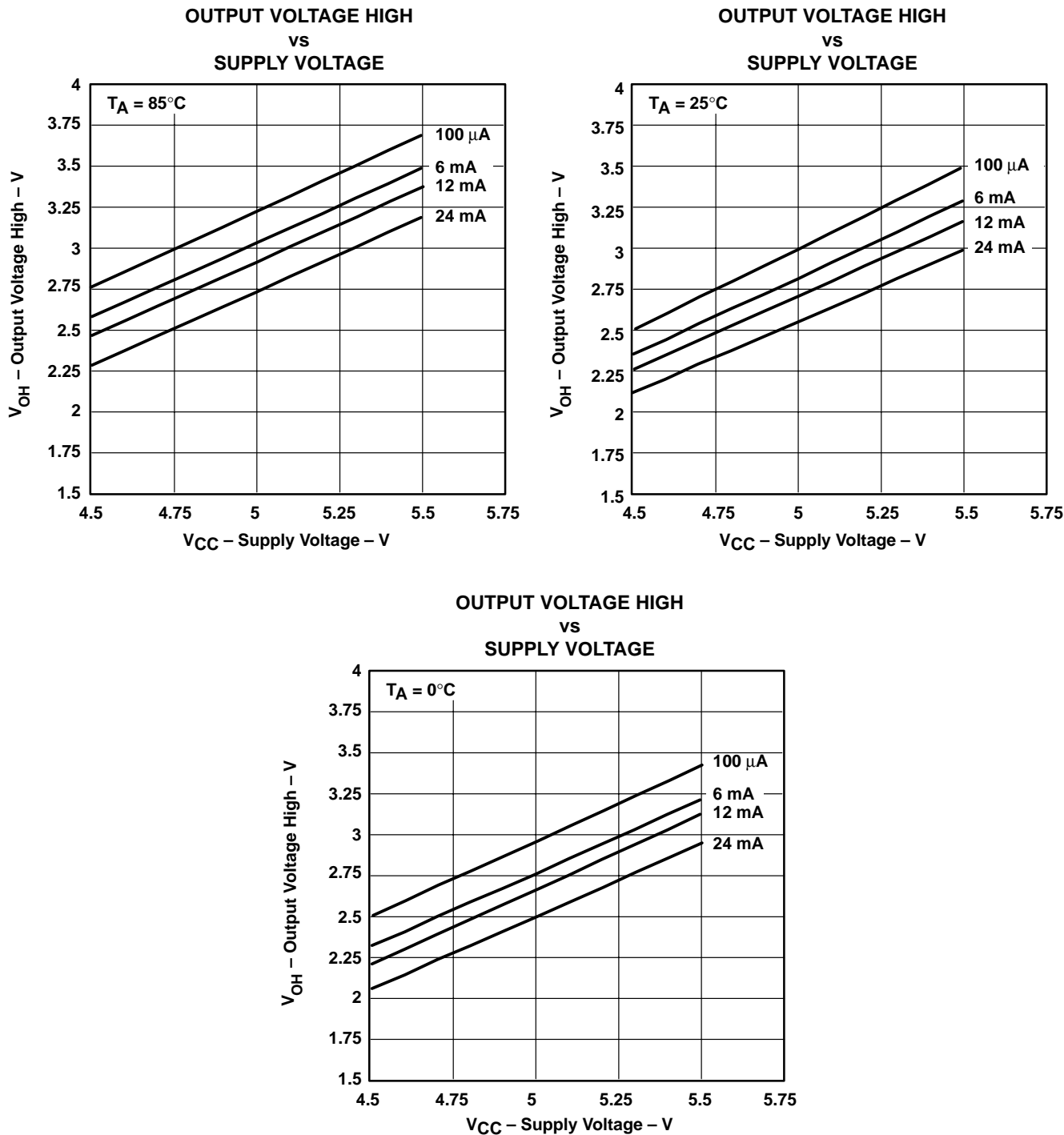**vs**
SUPPLY VOLTAGE

Figure 2. V_{OH} Values

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